REMARKS/ARGUMENTS

Claims 1-23 are pending in the application. Claims 1-23 are rejected. Claims 1, 11, and 22 have been amended for purposes of clarity.

Claims 1-4, 8-10, 11-16, and 20-22 were rejected under 35 U.S.C. §102(e) as being anticipated by Keller, U.S. Patent No. 6,636,959 (hereinafter "Keller"). Claims 5-7, 17-19, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Keller in view of "Register Renaming and Dynamic Speculation: an Alternative Approach," by Mayan Moudgill and Keshav Pingali (hereinafter "Moudgill").

Claim Rejections Under 35 U.S.C. §102(e)

Claims 1-4, 8-10, 11-16, and 20-22 were rejected under 35 U.S.C. §102(e) as being anticipated by Keller. Keller discloses a line predictor of cache alignment information for instructions (*See* Abstract).

Keller fails to teach or suggest determining a set of rename resources needed for said trace cache line on a per-packet basis based on relationships between the initial sequence of instructions, as recited in claims 1, 11 and 22. The Office Action responds:

> Finally, the line is terminated if the instructions within the line update a predefined maximum number of destination registers. This termination condition is set such that the maximum number of register renames that map unit 30 ***may*** assign during a clock cycle is not exceeded. In the present embodiment, 4 renames may be the maximum.

(Keller, Column 23, lines 22-27)(Emphasis added).

Keller discloses that a termination condition is set such that the maximum number of register renames that the map unit may assign during a clock cycle, the worst case scenario, is not exceeded. Keller does not disclose considering instances where the worst case scenario does

not occur, such as instances where interdependency between the instructions results in less than the maximum number of register renames being required.

Thus, an element of claims 1, 11, and 22 are not disclosed by Keller. Therefore, claims 1, 11, and 22 and by their dependency claims 2-4, 8-10, 12-16, and 20-21, are not anticipated by Keller.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 5-7, 17-19, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Keller in view of Moudgill. Moudgill discloses a mechanism implementing register renaming, dynamic speculation, and precise interrupts (*See* Abstract).

Neither Keller, Moudgill, nor any combination of the two teach or suggest determining a set of rename resources needed for said trace cache line on a per-packet basis based on relationships between the initial sequence of instructions, as claimed in claims 1, 11, and 22, and by their dependency claims 5-7, 17-19, and 23.

As stated above, Keller does not describe this element. Moudgill does not correct this deficiency. The Figure 1 of Moudgill, cited by the Office Action, describes simple renaming, and not consideration of the relationships between the instruction. Moudgill states:

> This serialization can be eliminated by renaming the result register of the (3), as shown in Fig. 1(b), so (3) can be executed in parallel with (1) and (2). Register renaming hardware attempts to apply this transformation dynamically, thereby increasing the amount of parallelism available.

(Moudgill, p. 202).

Moudgill is clearly discussing simple renaming and not determining a set of rename resources needed for said trace cache line on a per-packet basis based on relationships between the initial sequence of instructions.

Therefore, claims 5-7, 17-19, and 23, are not obvious under Keller in view of Moudgill.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

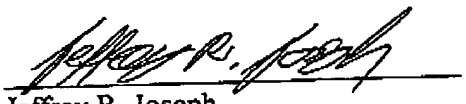
The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON LLP

Dated: February 13, 2006

By: 
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